REMARKS/ARGUMENTS

Reconsideration of this application is respectfully requested.

The rejection of all claims 1-9 as allegedly anticipated by Miki '244 is respectfully traversed.

The Examiner has merely paraphrased the applicant's claim language and then made general citations to portions of Miki which allegedly teach such paraphrased language – exactly (i.e., in an anticipatory manner). However, careful study of the passages referred to by the Examiner demonstrate that these passages fail to support such an allegation.

In a nutshell, one demonstration of this problem revolves around the fact that applicant's claimed invention requires determining a reduced or possibly even minimized delay for a "shortcut" for packet-switched traffic passing through a circuit-switched network when the ultimate destination node for the packet-switched traffic may not even itself be within the circuit-switched network. Miki is simply irrelevant to such minimized-delay shortcuts.

Miki relates to an IP switching network for providing communication between: (a) a frame-relay/IP network where data is carried in IP packets on a frame-relay carrier, and (b) an ATM/IP network where data is carried in IP packets on an ATM carrier.

The IP switching network of Miki comprises two classes of IP switches: a simple IP switch and an IP switch-with-multiplexer.

The IP switch with multiplexer comprises an ATM switch, an IP controller, a cell multiplexing-and-ATM switch is for switching ATM cells under control of the IP controller. The multiplexer/demultiplexer is connected between the ATM switch and the plurality of interfaces. In one direction cells received from the various interfaces are multiplexed and the cells thus multiplexed are transmitted to the ATM switch. In the other direction ATM cells received from the ATM switch in a multiplexed form are separated and then distributed to the respective interface. See Miki page 4, paragraphs [0073] – [0075].

The section of Miki referred to by the examiner describes receiving an IP data cell from an IP-over-frame-relay interface and deciding whether the IP data can be communicated by the redirection virtual circuit (VC). This is decided by assessing the amount of input data per constant time (i.e., data rate). Miki then goes on to describe how the redirect VC is set up (referred to as "add branch").

As set out at paragraphs [0009] – [0011] on page 4, Miki addresses the problem of the processing bottleneck of conventional IP processors. Miki is also concerned with reducing the delays in processing and transmitting IP packets. Miki responds to these problems by providing a different design of IP switch by adding a multiplexer and a series of interfaces for support of a plurality of communication protocols.

The applicant's claimed invention addresses a different problem and proposes a novel and non-obvious solution.

By way of contrast with the cited documents, the applicant addresses the problem of locating the most efficient route for passing packet traffic via a circuit switch network.

According to the applicant's claimed invention, a number of different gateways are investigated for possibly providing an interface between the circuit-switch network and the packet-switch network. This is not disclosed in any of the documents cited by the Examiner.

The presently claimed invention further describes a method requiring a plurality of such gateways to each probe a destination address in the packet switch network (e.g., to report to a controller on the delays experienced in obtaining a reply). One of the gateways is selected depending upon the delay times reported and establishes a virtual circuit to the selected gateway. None of the above steps are found in the documents cited by the Examiner.

The Examiner contends that Miki discloses at the indicated passages (i.e., page 6, paragraph [0113] to page 7 paragraph [0116] arranging a plurality of gateways to output polling messages and to determine the delay in receiving replies from respective target addresses. The Examiner also contends that Miki discloses selecting one of the gateways depending upon the respective delay times provided. However, upon careful reading of the passages indicated by the Examiner no indication can be found there of the above features. The Examiner is therefore asked to indicate precisely the wording in the text of Miki which is alleged to disclose any of the above features.

In the absence of such teaching in the prior art, the subject matter of claim 1 is clearly novel over the cited documents. By use of the novel method set out in claim 1, the applicant provides a communication system which maximizes the benefits to be obtained by the use of "cut-throughs" for packet traffic in a circuit-switch network, even when the ultimate destination of the packet does not itself lie in the circuit-switched network. This allows the optimum

destination point on the circuit-switched network for the cut-through to be selected dynamically to provide the best path to the destination packet address.

The applicant's invention advantageously allows a plurality of alternative routes through the circuit-switched network to be explored in order to identify that route which provides reduced or even minimum delay in communicating with a selected destination address in the target packet-switched network. These are significant advantages for which no indication can be found in the cited documents and are witness to the non-obviousness of the claimed invention.

Accordingly, this entire application is now believed to be in allowable condition and a formal Notice to that effect is respectfully solicited.

Respectfully submitted,

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